What is claimed is:

1. A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, wherein a target memory cell in the memory blocks is accessed according to an input bank address, row address, and column address, the semiconductor memory device comprising:

a row decoding section for decoding the row address so as to generate a row selecting signal; and

a column decoding section, adjacent to the row decoding section, for decoding the column address so as to generate a column selecting signal, and

wherein word lines driven by the row selecting signal and column selecting signal lines for outputting the column selecting signal are arranged parallel to each other in plan view ~~other~~, so as to supply these signals to the memory block of the target memory cell and to access the memory cell.

2. A semiconductor memory device as claimed in claim 1, wherein the column selecting signal lines are provided between the adjacent word lines.

3. A semiconductor memory device as claimed in claim 1, wherein the word lines and the column selecting signal lines are supplied to the memory block from the same direction.

4. A semiconductor memory device as claimed in claim 1, wherein the word lines and the column selecting signal lines are formed in the same wiring layer.

5. A semiconductor memory device as claimed in claim 1, wherein each word line has a hierarchical structure including sub word lines connected to the memory cells and a main word line which controls these sub word lines.

6. A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, wherein a target memory cell in the memory blocks is accessed according to an input bank address, row address, and column address, the semiconductor memory device comprising:

a row decoding section for decoding the row address so as to generate a row selecting signal;

a column pre-decoding section for pre-decoding the column address so as to generate a column pre-decoded signal; and

a column decoding section, provided in an area of the memory block where a sense amplifier for sensing the memory cell is provided, for performing the main decoding operation of the column address based on the column pre-decoded signal, and selecting the column on the memory block designated by the column address.

7. A semiconductor memory device as claimed in claim 6, wherein the column pre-decoded signal is supplied to the area where the sense amplifier is provided, for each bank.

8. A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, comprising:

a connecting portion, provided on each memory cell in the memory blocks, for connecting metallic wiring layers.

9. A semiconductor memory device as claimed in claim 8, wherein the connecting portion is a through hole.

10. A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, wherein a target memory cell in the memory blocks is accessed via input/output lines according to an input bank address, row address, and column address, the semiconductor memory device comprising:

a row decoding section for decoding the row address so as to generate a row selecting signal; and

a column decoding section for decoding the column address so as to generate a column selecting signal, and

wherein column selecting signal lines for outputting the column selecting signal and the input/output lines are arranged perpendicular to each other.

8 ~~11~~. A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, wherein a target memory cell in the memory blocks is accessed according to an input bank address, row address, and column address, the semiconductor memory device comprising:

a row decoding section for decoding the row address so as to generate a row selecting signal; and

a column pre-decoding section for pre-decoding the column address so as to generate 2-party column pre-decoded signals; and

a column decoding section, provided in an area of the memory block where a sense amplifier for sensing the memory cell is provided, for performing the main

decoding operation of the column address based on the column pre-decoded signals, and selecting the column on the memory block designated by the column address, and

wherein the area where the sense amplifier is provided is arranged between lines for outputting the 2-party column pre-decoded signals.

9 12. A semiconductor memory device as claimed in claim 8 11, wherein the 2-party column pre-decoded signals are supplied to the column selecting section from either side of the column selecting section.

13. A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks, wherein a target memory cell in the memory blocks is accessed according to an input bank address, row address, and column address, the semiconductor memory device comprising:

a row decoding section for decoding the row address so as to generate a row selecting signal;

a column pre-decoding section for pre-decoding the column address and the bank address so as to generate a column pre-decoded signal; and

a column decoding section, provided in an area of the memory block where a sense amplifier for sensing the memory cell is provided, for performing the main decoding operation of the column address based on the column pre-decoded signal, and selecting the column on the memory block designated by the column address.

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